REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Status of Claims

Claims 1-15 are present for examination.

Drawing Changes

Applicant is submitting herewith a new Figure 8 making a minor correction to indicate an arrow going into the scan flip-flop 32 from the parallel input pins PIN3. No new matter has been added.

Prior Art Rejection - James

Claims 1, 2, 3, 6-9, 12 and 13 stand rejected under 35 U.S.C. 102(b) as anticipated by James (5,678,289). The examiner points to Figures 6 and 8 of the James patent and equates the three multiplexes illustrated with applicant's recited first, second and third selecting means and further the examiner equates the temporary data storage section with the flip-flop 43 shown in James.

Arguments

The examiner's rejections are respectfully traversed.

In the structure of the present invention, three signals, that is, output signals from the first and second target circuits (to be tested) and a test signal (indicating a test pattern) are input and one of the three signals is selected, and the selected signal is temporarily stored and output as a test result. Therefore, as shown in Fig. 2, which is appended to the specification of the present application, a plurality of test circuits can be serially connected while each target circuit is placed between and connected to the first and second target circuits, and a test signal can be supplied from a dedicated test terminal to the test circuit at the head. Such structures can be further connected in parallel. In this case, the test signal can be supplied in

parallel (refer to test circuits 11 and 12 and test circuits 13 and 14 arranged between two cores and one user circuit in Fig. 2).

In each test circuit, a test signal or one of signals from a plurality of target circuits connected to the test circuit can be suitably selected as an input signal, thereby performing various kinds of tests for the target circuits.

Moreover, the examiner has ignored specific limitations in applicant's independent claims 1 and 9. For example, in reference to claim 1, applicant recites a first selecting section (10-1) for selecting and outputting one of a first output signal output from the first target circuit, a second output signal output from the second target circuit and a test signal indicating a test pattern input via a test pattern input terminal according to a first and second test mode signals supplied from an exterior device. The first output signal from the first target circuit is supplied at terminal co; the second output signal from the second target circuit is supplied to terminal ui, and the test signal indicating the test pattern is supplied to terminal si. Thus, three separate inputs are fed to the first selecting circuit and the output of same is determined by a first test mode signal, S, and the second test mode signal T. Even at this stage of applicant's recitation, James fails to disclose applicant's recited structure. The MUX 41 of James (Figure 6 or Figure 8) has only two inputs thereto and is controlled by only a single selection input. Thus, James' structure is quite different from applicant's recited structure.

Going further, applicant next recites, again in reference to claim 1, the temporary data storage section for temporarily storing the signal selected by the first selection as a data signal. Applicant's flip-flop 10-2 is analogous to James' flip-flop 43.

Applicant goes on to recite a second selecting circuit for selecting one of the temporarily stored data signals or the second output signal from the second target circuit according to the second test mode signal. Thus, applicant specifically recited the second test mode signal, T, is fed to applicant's second selector circuit 10-3. This signal selects either the output of the flip-flop 10-2 or the output from the second target circuit. While James shows a MUX 47 connected by an intermediate flip-flop 45 to the output of the storage flip-flop 43, the selection signal utilized by James is a mode selection signal which is different

from the single "SHIFTDR" signal fed to James' first multiplexer 41. Thus, again, applicant's recited structure is clearly not shown by James.

Finally, applicant recites a third selecting section for selecting one of the temporarily stored data signals or the first output signal from the first target circuit according to a third test mode signal. While James has indeed a third multiplexer 66, and the output of the flip-flop 43 as well as the output of a serial data input are fed thereto, it appears that the select signals on line 59 to the multiplexer 66 are determined, at least in part by flip-flop 43.

As may be seen, there are many structural differences between the recitation as set forth in applicant's claim 1 and the James structure shown in Figure 6 or 8. Similar reasoning applies to independent claim 9. As such, applicant's independent claims 1 and 9 are clearly not anticipated by the James reference, and the section 102 rejection must be withdrawn. Applicant's dependent claims 2, 3, 6, 7, 8, 12 and 13 depend directly or indirectly upon independent claims 1 and 9 and are likewise deemed patentable at least for the same reasons indicated above with regard to the independent claims from which they depend.

Prior Art Rejection - Asaka

Claims 4, 5, 10, 11, 14 and 15 stand rejected under 35 U.S.C. 102(e) as being anticipated by Asaka (6,189,128). The examiner equates the first calculator 651 of Asaka with applicant's parallel number calculating section and the second calculator 652 with applicant's serial length calculating section.

Argument

The examiner's rejections are respectfully traversed.

In the structure of Asaka, one of the first and second candidates (calculated by the calculators I (651) and II (652)) of each of a plurality of appropriate paths is selected by the path selector 653, where the selected candidate has a smaller occupied area. In contrast, in the present invention, the parallel number (which indicates the number of input-output chains, each chain for inputting and outputting a test signal) and the serial length (calculated

by using the parallel number and the number of terminals of the target circuits), respectively calculated by the parallel number calculating section and the serial length calculating section, are not compared so as to select and use one of the calculated results, but both calculated results are used so as to produce test circuits for testing target circuits in an integrated circuit device.

Therefore, the present invention clearly differs from the structure disclosed by Asaka.

Moreover, in accordance with the description of Asaka, the intent is to provide a design for a testing method and device that can minimize area overhead in the occupied area of a circuit. In accordance with the teaching set forth in column 10, the first calculator 651 reads as appropriate the occupied areas of the various circuit elements that had been registered beforehand in the circuit element library 62. The calculator then calculates each of the occupied areas in order to form a first-candidate scan pass by connecting control elements to the control terminals of multiplexers in appropriate paths that include a multiplexer. The second calculator 652 also reads the occupied areas of the various circuit elements that have been registered beforehand in the circuit element library 62 and calculates each of the occupied areas for cases of forming a second-candidate scan path by replacing each register of a plurality of appropriated paths by a scanned element. The first calculator 651 calculates the occupied areas of the first candidate scan paths by connection control elements to the control terminals of multiplexers similar to the second prior art method described in the background section of Asaka.

In contrast, applicant's invention does not calculate occupied areas and does not have as its objective a minimization of area as an overhead item.

In contrast, applicant's invention is based on the structure of the user circuits, and parallel test terminals. For example, in reference to claim 4, applicant's parallel numbered calculating section calculates the number of input-output chains. This number is based on the number of test terminals for connecting the integrated circuit device with external circuits. The parallel number indicates the number of pairs of the input and output terminals of the parallel test terminal. The parallel number can thus be determined by dividing the number of

parallel test terminals by 2. In reference to applicant's Figure 2, there are 4 parallel test terminals and dividing by 2 results in a parallel number of 2.

Applicant's claim 4 goes on to recite a detecting section for comparing the number of input terminals and the number of output terminals of each target circuit in determining a larger or equal number as a compared result. Again, in reference to applicant's Figure 2, looking at core 2, one notices a total of 7 input and output terminals. (The number of input terminals is 4 and the number of output terminals is 3). Thus, the number of input terminals is divided by the parallel number determined above with the calculated results being 2. As a result of the parallel number calculating section and the serial length calculating section, the number of input-output chains for parallel-testing each target circuit is determined based on the parallel number calculated by the parallel number calculating section and the serial length of each input-output chain determined based on the serial length for the relevant target circuit calculated by the serial length calculating section.

No such teaching is found in Asaka, and thus Asaka cannot form an anticipatory reference under 35 U.S.C. 102. In order for a reference to anticipate a claim, the reference must disclose each and every limitation of the recited invention.

The examiner's rejection of applicant's remaining independent claims 5, 10, 11, 14 and 15 is similar to the examiner's rejection of claim 4 in equating the first calculating section (or calculating step) and second calculating section (or calculating step) with Asaka's first and second calculators respectively. However, as indicated above, this correspondence is entirely incorrect as applicant's parallel number calculating section and serial length calculating section are quite different from the first and second calculators of Asaka. As such, the section 102 rejection must be withdrawn, and it is submitted that applicant's claims 5, 4, 10, 11, 14 and 15 are patentable over the prior art.

In view of the arguments set forth above and the amendments made hereto, it is submitted that the application is now in condition for allowance and an early indication of same is earnestly solicited.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

Date 7-21-03

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